(12) UK Patent Application (19) GB (11) 2 215 925 (13) A

(43) Date of A publication 27.09.1989

(21) Application No 8903435.9

(22) Date of filing 15.02.1989

(30) Priority data
(31) 8803431 (32) 15.02.1988 (33) GB

(51) INT CL⁴
H03M 1/74

(52) UK CL (Edition J)
H3H HBA H1X

(56) Documents cited
EP 0135274 A2

(58) Field of search
UK CL (Edition J) H3H HBA
INT CL⁴ H03K, H03M

(71) Applicant
Marconi Electronic Devices Limited

(Incorporated in the United Kingdom)

Doddington Road, Lincoln, LN6 3LF, United Kingdom

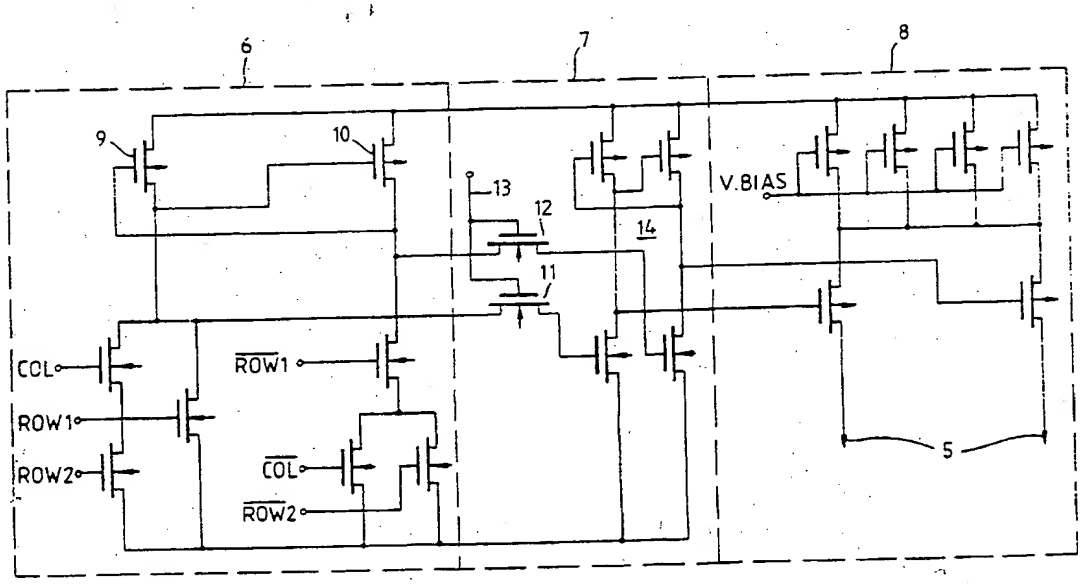
(72) Inventors
Alexander William Vogt
Ian Juso Dedic

(74) Agent and/or Address for Service
C. F. Hoste
The General Electric Company p l c, GEC Patent Dept
(Wembley Office), Hirst Research Centre, East Lane,
Wembley, Middlesex, HA9 7PP, United Kingdom

(54) Digital to analogue converter

(57) A high-speed digital to analogue converter comprises a matrix of cells each including a current source 8, in which there are provided means 7 within each cell to bring into operation simultaneously all those current sources required to decode any one value.

Fig. 2.



GB 2 215 925 A

Fig.1.

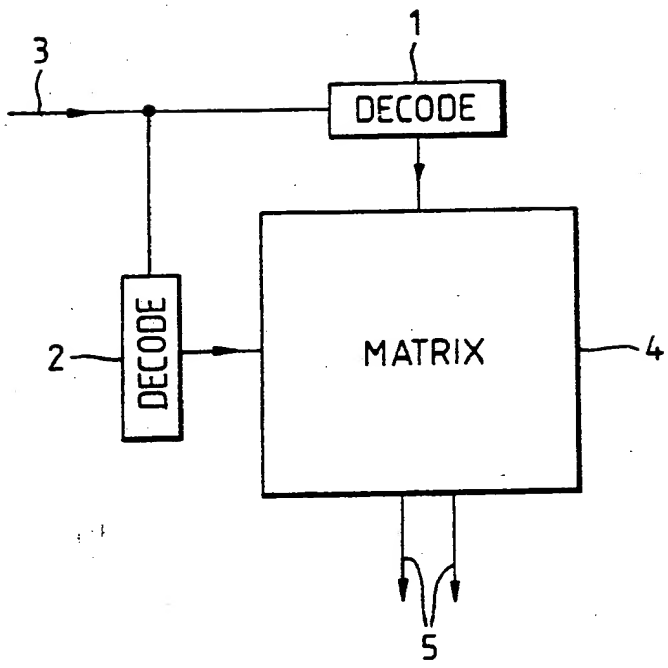
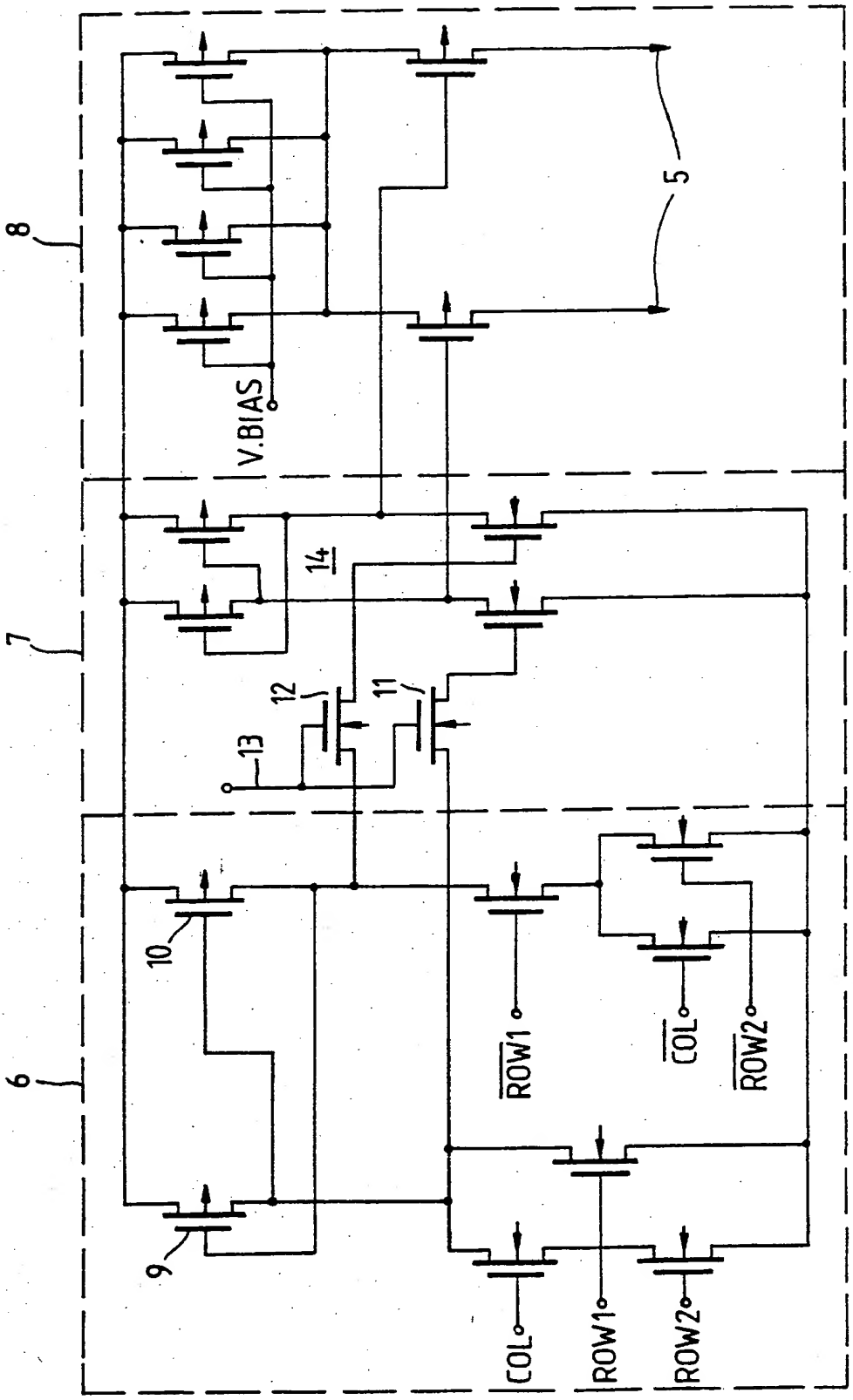


Fig. 2.



SC/3290

Digital to analogue convertors.

The present invention relates to digital to analogue convertors.

A high speed digital to analogue convertor for, say, video applications may comprise an array or matrix of substantially identical current sources all having their outputs connected in common to the output of the convertor. Digital decoding circuits are utilised to determine how many of the sources are brought into operation in response to any one digitally coded input signal to produce a total analogue output current of the appropriate magnitude. The decoding circuits must allow each source in the matrix to be accessed.

The matrix may be made up of a set of cells each comprising local decoding, control circuitry and a current source, and these cells may be addressed by means of column and row decoding circuits.

Known decoders of this form suffer from the effects of different delays in the various decoding paths between the digital signal input and the respective current sources, because of which the current sources switch on or off at different times, causing glitches on the output path during transitions between input codes, settling problems and output transients that are dependent upon the input codes.

According to one aspect of the present invention in a digital to analogue convertor comprising a plurality of current sources each arranged selectively to supply a current of a predetermined magnitude to a common output path and means to enable a respective number of said current sources in dependence upon the value represented by a digitally coded input signal to said convertor, there are provided means associated with each of said current sources to bring into operation substantially simultaneously all of said sources that are so enabled.

According to another aspect of the present invention a digital to analogue convertor comprises a matrix of cells each including a respective current source and respective switching means, each of said current sources being arranged selectively to supply a current of a predetermined magnitude to a common output path upon operation of the respective switching means, and means selectively to enable a plurality of said current sources in dependence upon a value represented by a digitally coded input signal to said convertor.

The convertor may comprise an array or matrix of cells each comprising one of said current sources and respective switching means by which the respective current source may be brought into operation. Each cell may also include respective decoding means by which the respective current source may be enabled in response to appropriate digitally coded input signals.

A digital to analogue convertor in accordance with the present invention will now be described by way of example with reference to the accompanying drawings, of which:-

Figure 1 shows the convertor schematically, and

Figure 2 shows diagrammatically part of the convertor of Figure 1.

Referring first to Figure 1 the convertor comprises column decoding means 1 and row decoding means 2 responsive to a digitally coded input signal on an input path 3 to bring into operation a number of current sources (not shown) in an array or matrix 4 to produce on an output path 5 a current of a magnitude dependent upon the value represented by the digitally coded input signal. The matrix 4 may

comprise, say, 64 cells (not shown) each including a current source, to enable the digital to analogue conversion of a six-bit linearly coded input signal.

Referring to Figure 2, each cell comprises a local decode circuit 6, a switch drive circuit 7 and a current source 8. As shown, the decode circuit 6 is responsive to one column address bit and its inverse and two row address bits and their inverses to set the condition of a pair of cross-coupled p-channel devices 9 and 10.

During transitions between one coded input signal and the next, while the row and column and local decoding circuits are settling, a pair of series n-channel devices 11 and 12 are switched to a non-conducting condition by means of a control signal applied in common to all cells of the matrix by way of a path 13, and a half-latch circuit 14 maintains the current source 8 in its existing state. Once the decoding circuits have settled the devices 11 and 12 in all cells are switched into conduction substantially simultaneously by way of the path 13, whereby the half latches 14 and the current sources 8 in all cells are switched substantially simultaneously to the condition required by the new digitally coded input signal.

The combination of circuits shown in Figure 2 produces a structure with a minimum number of p-channel devices and n-p cross-overs, compact layout and a minimum capacitance loading on control and decode paths.

Integral non-linearity may be reduced, at the expense of differential non-linearity, by interleaving the signals selecting specific rows or specific columns. Instead of selecting rows, for example, in the order, 1,2,3,4,5,6,7,8 they may be selected in the order 4,5,3,6,2,7,1,8, and the same for the columns. This interleaving reduces the effects of gradients of properties across the matrix. It can also be regarded as randomising the selection of individual current sources.

The switching of all current sources together results in minimal glitches and transients which in general are not code-dependent.

As shown in the drawing the current sources produce both the required current and its inverse or complement, the latter being applied to a dummy load, in order to even out the current loading on the power supply.

CLAIMS

1. A digital to analogue convertor comprising a plurality of current sources each arranged selectively to supply a current of a predetermined magnitude to a common output path and means to enable a respective number of said current sources in dependence upon the value represented by a digitally coded input signal to said convertor, wherein there are provided means associated with each of said current sources to bring into operation substantially simultaneously all of said sources that are so enabled.

2. A digital to analogue convertor in accordance with Claim 1 comprising an array or matrix of cells each including one of said current sources and respective switching means by which the respective current source is brought into operation.

3. A digital to analogue convertor in accordance with Claim 2 wherein each cell includes respective decoding means by which the respective current source may be enabled in response to appropriate digitally coded input signals.

4. A digital to analogue convertor comprising a matrix of cells each including a respective current source and respective switching means, each of said current sources being arranged selectively to supply a current of a predetermined magnitude to a common output path upon operation of the respective switching means, and means selectively to enable a plurality of said current sources in dependence upon a value represented by a digitally coded input signal to said convertor.

5. A digital to analogue convertor in accordance with Claim 4 wherein there are provided means to address the cells of said matrix by rows and columns to enable a said plurality of said current sources.

6. A digital to analogue convertor in accordance with Claim 5 wherein each cell of the matrix includes means responsive to at least two row and column address signals selectively to enable the respective current source.

7. A digital to analogue convertor substantially as hereinbefore described with reference to the accompanying drawings.

Published 1969 at The Patent Office, State House, 66/71 High Holborn, London WC1R 4TP. Copies may be obtained from The Patent Office. Sales Branch, St Mary Cray, Orpington, Kent BR5 3RD. Printed by Multiplex techniques ltd, St Mary Cray, Kent, Con. 1/87